Using 60Hz Power Line Frequency as an Accurate Real Time Clock Timebase

Application Note | August 3, 2007 | AN1342.0

Introduction

Real Time Clock (RTC) devices contain an oscillator and normally require a crystal to operate with the required accuracy. Crystal oscillators are a good solution in that they provide high accuracy (<20ppm at +25°C), low cost and low power, but the one drawback is nonlinear temperature drift. That temperature drift is parabolic in nature, becoming progressively worse as the crystal temperature deviates from +25°C. For example, 100ppm drift will result in 1 minute of error per week. If high accuracy over temperature is required, then the oscillator needs to have temperature compensation included, necessitating some form of TCXO. This increased complexity leads to a more costly solution.

One way to provide an RTC solution with a fairly high degree of accuracy over-temperature is to use an external, very accurate clock source. The AC power in the U.S. and Europe is such a source, with either 60Hz or 50Hz frequency that is extremely stable over long time periods as well as over- temperature. Many devices using RTC's have access to AC power, and with some basic circuitry, can use this power source as a fundamental clock source.

Solution Overview

The main idea of the circuit is to convert the 60Hz power (using the U.S. as an example) to a useable clock source. That clock source must then be converted into an appropriate clock input for an RTC device. The input of most RTC devices is the common 32.768kHz crystal oscillator, which is internally divided to provide a one second clock. The RTC does not accept a 60Hz clock, so a PLL is needed to correct the frequency input for the RTC. Moreover, the 60Hz clock is not a submultiple of 32,768, so it needs to be divided down to a common factor before entering the PLL.

A block diagram is shown in Figure 1 which includes these functions. The low frequency clock synthesizer uses the 60Hz input as a reference clock, divides down to 4.0Hz for the PLL input, and outputs the 32.768kHz clock. The RTC uses that clock and divides it down to 4.0Hz internally as the error clock for the PLL phase detector.

Circuit Description *(See Figure 2)*

Input Clock Conversion

This application circuit uses a wall transformer for the AC line input. Since a clock input is needed, any transformer that produces a minimum of $4V_{P-P}$ sine wave can be used. The test circuit used a $9V_{RMS}$ or $30V_{P-P}$ AC signal, thus the circuit values were optimized for that output with 50% variation. This input is differential in nature, so the circuit ground is separated from the input with a 1.2kΩ resistor. This serves to limit input current and minimize ground variations. The sine wave input is half-wave rectified and then drives a diode to generate a square wave output.

Circuit values are established to keep current draw to a minimum while assuring a decent clock edge for the CMOS logic interface. Capacitor C_1 was added to soften transistor turnoff and minimize ringing. This circuit can handle a wide range of AC voltages and still yield a reliable clock signal, providing the consistent rising edge required for the PLL.

60Hz Clock Divider

A CMOS, programmable, clock-divider chip, the MC14526B, is used as a divide-by-15 circuit. It is programmed to start at a count of 15 and resets at 0. The MSB counter output used is a CMOS output at 4.0Hz at 50% duty cycle and is the reference clock input to the PLL chip. Note that 50Hz could also be used, but the divider will need to be set to 25 (involving a second counter IC or a single larger counter device) and the PLL input is then 2.0Hz.

PLL, VCO and Filter

An integrated PLL chip, the MC14046, based on the popular 4046 CMOS device, is used to generate the 32.768kHz clock for the RTC. There is a plethora of design information available for the PLL design. The VCO and filter design sections require some initial design considerations as well as in-circuit testing and adjustment as the components can exhibit up to 20% variations. The AC power line frequency is actually quite stable. While it may experience accumulated variations of ±500ppm, the offset does not vary instantaneously and, over long term, averages to zero.

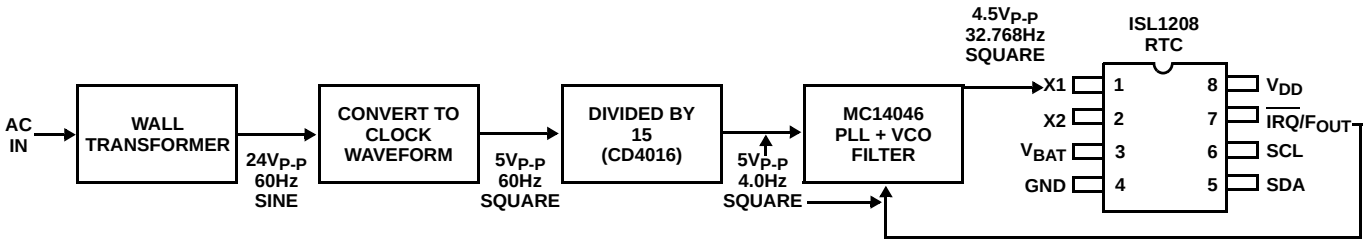

FIGURE 1. 60Hz RTC SIMPLIFIED BLOCK DIAGRAM

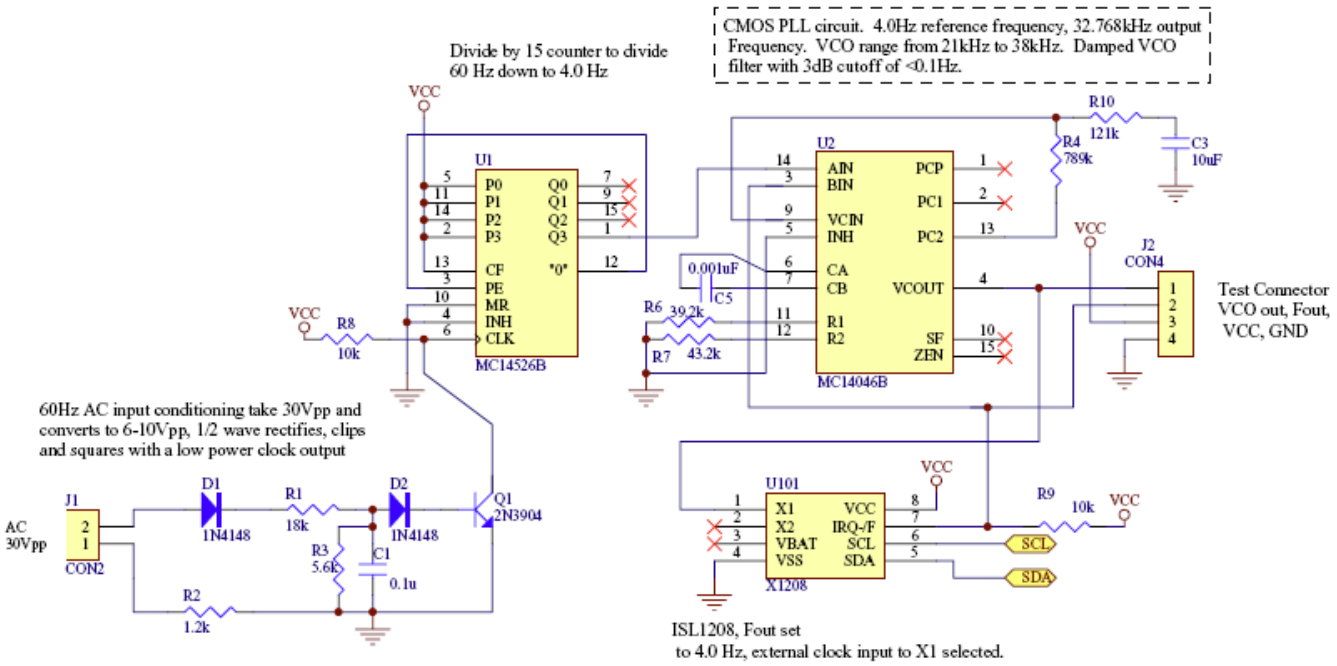

FIGURE 2. 60Hz RTC SCHEMATIC

Because of the long term stability, there is no need to follow large input frequency variations or to quickly settle. This is desireable since the 4.0Hz input clock frequency doesn't allow for a fast loop time constant.

Discrete components C_5 and R_6/R_7 set the VCO frequency range at 20.1kHz to 38.9kHz (referred to as f_{MIN} and f_{MAX}). Target values were 22kHz and 44kHz, and the measured values are fairly close with allowances for IC process and capacitor tolerance. R_6 and R_7 are 1% values, selected as metal film which provides the lowest temperature drift. This range gives enough range to lock yet limits the loop gain, improving stability. The VCO frequency output is a CMOS clock centered at 32,768Hz and is routed to the input of the RTC device (X1 pin).

The type 2 PLL phase detector is used, a sequential logic state machine which seeks to produce a zero phase error. R_4, R_{10} and C_3 form the PLL filter. This filter includes damping (R_4) to aid in settling and discourage oscillations sometimes associated with this type of PLL. Initial values for these components were chosen to give filter corner frequency (f_C) of <0.02Hz. Also, the ratio R_4:R_5 must be between 5:1 and 10:1 for loop stability, placing the zero well below the unity gain loop frequency. Equation 1 for f_C is:

$$f_C = \frac{1}{2\pi((R4 + R10)C3)} \quad \text{(EQ. 1)}$$

C_2 was set to 10µF, and the ratio R_4 = 6.5 x R_{10} was chosen, yielding R_4 =120,000 (121kΩ), and R_{10} = 780,000 (781kΩ). This results in:

f_C = 0.017Hz (pole), and

$$f_2 = \frac{1}{2\pi(R4 \cdot C3)} = 0.13\text{Hz} \quad \text{(EQ. 2)}$$

which is the 0.

Using the equations in the MC14046 data sheet, the other characteristics of the PLL were calculated:

$$K\Phi = V_{DD}/(4\pi) \quad \text{(EQ. 3)}$$

$K\phi$ = 0.40 V/r

$$K_{VCO} = \frac{2\pi\Delta f_{VCO}}{V_{DD} - 2V} \quad \text{(EQ. 4)}$$

Note that Δf_{VCO} = 38.9 - 20.1 = 18.8kHz, so:

K_{VCO} = 39,374 r/s/V

The equation for the natural frequency ω_n is:

$$\omega_n = \sqrt{\frac{K\Phi \cdot K_{VCO}}{N \cdot C3 \cdot (R4 + R10)}} \quad \text{(EQ. 5)}$$

where N = 8192, giving:

ω_n= 0.46 r/s

The damping factor is in Equation 6:

$$\zeta = 0.5\omega_n \cdot \left(R4C3 + \frac{N}{K\Phi K_{VCO}}\right) \quad \text{(EQ. 6)}$$

Yielding ζ = 1.93. This value is much higher that the 0.7 value typically desired. Iterations of the design equations do not yield any improved soltions, so bench testing was used to evaluate the characteristics of the circuit.

RTC Operation

The ISL1208 device was chosen for the Real Time Clock function. It contains RTC counters and registers, a single alarm, a programmable clock frequency output and an I^2C interface for communications. Note that the clock frequency

output pin can also be used for alarm interrupts. If the clock output function is enabled, the interrupt capability is disabled.

The ISL1208 has battery backup capability as well, which is not necessarily important in this application. A backup lithium cell or supercapacitor can be connected to the V_{BAT} pin, but it would only be useful for retaining the contents of the SRAM registers since loss of main power would most likely result in loss of the clock source (AC power) as well.

The ISL1208 contains crystal connection pins X1 and X2. The X1 pin can also be programmed for an external clock via the XTOSCB bit in the Status register (bit 6 of register address 07h). When this bit is set to 1 the oscillator is disabled and X1 is a CMOS-compatible clock input. This Status register also has the function of enabling/disabling I^2C write functions. Therefore, any time a write to the status register is performed, bit 6 must also be reset to 1 or clock counting ceases.

Register 08h, the INT register, contains 4-bits for setting the output clock frequency, ranging from 1/32Hz to 32,768Hz. The clock output needs to be set to 4.0Hz for this application which is x8h (the other bits are free for other user to set other functions). When the circuit is first powered up, these two registers must be set correctly before the clock/calendar data is entered or the time will not advance and the clock will be inaccurate. To summarize Table 1 shows the register settings:

TABLE 1. REGISTER SETTINGS

REGISTER	FUNCTION	BIT SETTING
07h	Status Register	xx1xxxxxb
08h	INT Register	xxxx1000b

(x = bits can be set according to other functions)

Test Results

The circuit was built on a small prototype PC board, attached to the ISL1208 daughtercard, and used with the Intersil USB RTC evaluation board. Board power was applied first, then the AC input applied. The registers were set up per the directions in the RTC section and the VCO output was monitored with a frequency counter. Since the time constant for the PLL is relatively long, on the order of 10's of seconds, it is best to program the clock/calendar information after settling to prevent losing initial clock accuracy.

Measurements were taken of initial settling using the VCO output, shown in Figure 3. Settling occured within 30s or so, with the time constant consistent with the design target. Measurements were also taken long term by monitoring the real time clock seconds and comparing to a PC computer clock, set to the NIST-provided reference time. Over a period of 2 weeks the deviation varied ±2 seconds, but never greater, which agrees with the published accuracy for power line frequency in the US. Short term measurements on the 60Hz frequency show that it can deviate more than this (up to ±500ppm over a period of hours) but averages to zero over a longer time period (1 week), There is no cumulative error over long periods with the AC input as a frequency source.

The circuit was placed in a temperature chamber to test the high and low temperature performance. This is where crystals are problematic since the parabolic temperature curve results in up to -160ppm of frequency drift (at -40°C), resulting in cumulative error. Not all crystals are specified for the full -40°C to +85°C industrial temperature range as well.

The VCO output was monitored while the circuit was heated to +85°C for one hour and cooled to -40°C for 30 minutes. No excess frequency deviation was observed (<500ppm magnitude) from 4.0000Hz and the RTC time stayed within +1s error during both tests. Care was taken handling the board during these tests to insure no loss of power or clock happened which could skew the results.

Conclusion

The circuit designed and assembled using 60Hz power for RTC clocking proved to have very good long term accuracy. Unlike crystals, the 60Hz source has no temperature dependencies although exhibits some short term drift. Products that utilize RTC devices and rely on AC powered systems can use this type of solution to produce a reliable and accurate clock, avoiding many of the drawbacks inherent with a crystal circuit. This circuit provides an accurate and reliable time of day over the long term, needing an update only when the AC power is lost.

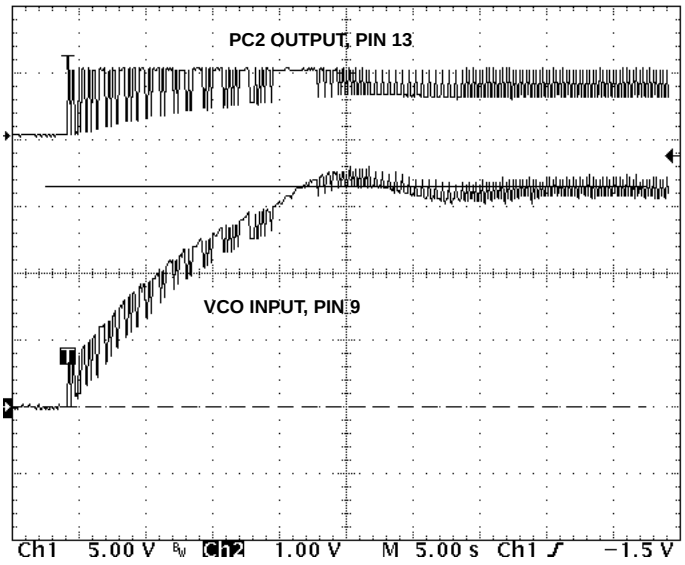

FIGURE 3. STARTUP RESPONSE FOR THE PLL CLOCK